region of an NMOS (N-channel metal oxide semiconductor) transistor to the power supply voltage VDD and the ground potential VSS, respectively.

IN THE CLAIMS:

Please amend claims 1 and 8, and add new claims 19-20 as follows:

1. (Once Amended) A fundamental cell, used as a basic unit in layout of a semiconductor integrated circuit device and being in a stage after metal wiring is formed, comprising:

no fixed wiring for commonly wiring between fundamental cells, and

connector terminals to be connected to upper wiring layers.

8. (Once Amended) A semiconductor integrated circuit device, comprising:

a fundamental cell, used as a basic unit in layout and being in a stage after metal wiring is formed, having no fixed wiring to be commonly wired between the basic units, and having connector terminals to be connected to upper wiring layers; and

upper wirings in predetermined wiring directions and in predetermined wiring widths both appropriately selected, for connecting, in the upper wiring layers, the corresponding connector terminals of the fundamental cell.

-- 19. (New) A fundamental cell according to claim 1, wherein the metal wiring includes at least one of a power wiring and a wiring in a function block.

20. (New) A semiconductor integrated circuit device according to claim 8, wherein the metal wiring includes at least one of a power wiring and a wiring in a function block. --